CLOCK SIGNAL GENERATORS HAVING PROGRAMMABLE FULL-PERIOD CLOCK SKEW CONTROL AND METHODS OF GENERATING CLOCK SIGNALS HAVING PROGRAMMABLE SKEWS

Abstract of the Disclosure

Clock signal generators include an integrated circuit chip having a PLL-based or DLL-based clock driver therein. The clock driver is configured to support generation of a plurality of clock signals having different frequencies in a range between 1 and 1/N times a frequency of an internal clock signal and full-period programmable skew characteristic, where N is a positive integer greater than one. The clock driver also includes a divide-by-N clock generator that is configured to generate N divide-by-N clock signals that have the same frequency but are phase shifted relative to each other. This clock generator operates in response to a first skew signal having a frequency equal to the frequency of the internal clock signal. A one-of-N select circuit is provided. This select circuit is configured to select one of the N divide-by-N clock signals in response to a time unit position signal. A synchronization unit is electrically coupled to an output of the divide-by-N clock generator circuit and is synchronized to the first skew signal. The synchronization unit is also coupled to an output buffer that is configured to drive an off-chip load with the selected divide-by-N clock signal having the desired skew characteristic.

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